REMARKS

Claims 1-31 are pending in this application. Claims 1-31 stand rejected. Claims 1, 14, 19, and 26-31 have been amended. Claims 1-31 remain in the application. Applicant respectfully traverses the rejections for the reasons expressed herein below.

A. Rejection of Claims 1-5, 14, and 16-18 under 35 U.S.C. § 103(a)

Claims 1-5, 14, and 16-18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over prior art Figure 9 in view of United States Patent Nos. 5,861,345 and 5,656,337, issued to Chou et al. ("Chou") and Park et al. ("Park"), respectively. Applicant respectfully traverses this rejection and requests reconsideration of claims 1-5, 14, and 16-18.

Claims 1-5, 14, and 16-18, as amended, recite a method of forming a dielectric layer having an opening with an aspect ratio greater than about two. A first dielectric layer is formed in the opening wherein a portion of the opening not filled with the first layer has an aspect ratio of not greater than about two. A second dielectric layer is formed over the first layer filling the portion of the opening not filled with the first dielectric layer, and has a top surface that is not within the opening.

As stated on page 6, lines 10-14, a problem exists in the art in that openings having aspect ratios greater than about two are difficult to fill at relatively high deposition rates and often suffer from shadowing effects. The present invention substantially addresses this problem because it provides good gap-fill characteristics, even at high aspect ratios of greater than about two. In particular, it has been found that the first dielectric layer may be formed at a relatively low deposition rate, when the impingement rate is low, so that voids between the structures, due to the shadowing effect, are either eliminated or greatly reduced. As a result, the first dielectric layer provides improved protective, insulating and

capacitive qualities in the critical gap areas or openings between the structures in order to protect the circuit from impurities, moisture, and stress related impacts. The second dielectric layer may then be formed at a deposition rate higher than the first dielectric layer.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the combination of prior art. MPEP §2143.03. In addition, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. MPEP §2143. Put another way, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination or modification. MPEP §2143.01. In addition, it must be remembered that a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. MPEP §2141.02.

As set forth on page 2 of the specification, prior art FIG. 9 illustrates a dielectric formation problem known in the art known as "shadowing", wherein some areas in the openings 118 between the structures 112 are more prone to developing voids 110 during the formation of the dielectric layer 102, thereby resulting in a less effective integrated circuit. As illustrated in FIG. 9, and as discussed throughout the specification, the "shadowing" effect prohibits the formation and filling of the first dielectric layer in the opening.

It is respectfully submitted that prior art FIG. 9 cannot form the basis of a rejection of claims 1-5, 14, and 16-18 under 35 U.S.C. § 103(a). As illustrated in FIG. 9, and as discussed throughout the specification, the "shadowing" effect inhibits the formation of the first dielectric layer (and successive other dielectric layers) in the opening. As a result, the voids that are formed as a result of "shadowing" do not allow the first or successive

dielectric layers to fill the opening. In order to clarify claims 1-5, 14, and 16-18 of the present invention, each of the independent claims has been amended to more specifically claim that the combination of the first and the second dielectric layer fill the opening. It is asserted that prior art FIG. 9 only describes the problems found in the prior art. FIG. 9 provides no solution to the "shadowing" effect, nor does it teach or suggest a method of filling an opening on or in a substrate through the formation of a first and second dielectric layer, as recited in claims 1-5, 14, and 16-18 of the present invention.

Furthermore, nothing in Chou, when combined with prior art FIG. 9, teaches of suggests the method of forming a dielectric layer as recited in claims 1-5, 14, and 16-18. Chou discloses an *in situ* inter-dielectric process for forming multilevel metal structures on a semiconductor. The method comprises forming an SOG layer on an uneven semiconductor surface, treating a surface of the SOG layer with a plasma in a PECVD chamber, and forming a PECVD layer on the treated surface in the same PECVD chamber.

It is asserted that Chou does not teach or suggest, either alone or in combination with prior art FIG. 9 and/or Park, the method recited in the present invention. Specifically, Chou does not teach or suggest a method of forming a dielectric layer in an opening with an aspect-ratio greater than about two, wherein the first dielectric layer is formed in the opening such that a portion of the opening not filled with the first layer has an aspect ratio of not greater than about two, and wherein the second dielectric layer is formed over the first layer filling the portion of the opening not filled with the first dielectric layer, and has a top surface that is not within the opening. Indeed, the Examiner only relies on Chou for teaching the formation of a second dielectric layer over a first dielectric layer, with the top surface of the second layer not within the opening, and the use of a silicon substrate.

Furthermore, nothing in Park, when combined with prior art FIG. 9 and Chou, teaches of suggests the method of forming a dielectric layer as recited in claims 1-5, 14,

and 16-18. Park discloses a method of forming a planarized dielectric layer for a semiconductor device that is formed between a metal wire conductive layer or an interlayer prior to metallization. A conductive layer and the underlying layer are surface treated to have different electrical polarities so that the dielectric is formed by using the difference of deposition rates of the dielectric material between that of the conductive layer and that on the underlying dielectric. Park, like Chou, it not directed to the method recited in claims 1-5, 14, and 16-18. Indeed, the Examiner only relies on Park for teaching the formation of a dielectric layer with one deposition rate greater than another deposition rate.

Accordingly, in view of the amendments made to the claims and the supporting arguments set forth above withdrawal of the rejection to claims 1-5, 14, and 16-18 under 35 U.S.C. § 103(a) over prior art FIG. 9 in view of Chou and Park is respectfully requested.

B. Rejection of Claim 15 under 35 U.S.C. § 103(a)

Claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over prior art Figure 9, Chou, and Park as applied to claims 1-5 above, and further in view of United States Patent No. 5,909,044, issued to Chakravarti ("Chakravarti"). Applicant respectfully traverses this rejection and requests reconsideration of claim 15.

For at least the reasons discussed above that distinguish claims 1-5, 14, and 16-18 from the combination of teachings of prior art FIG. 9, Chou, and Park, it is believed that claim 15, that is dependent from claim 14, is also distinguishable from FIG. 9, Chou, and Park.

Furthermore, nothing in Chakravarti, when combined with FIG. 9, Chou, and Park would render claim 15 obvious. Chakravarti teaches a method of forming an integrated circuit that includes obtaining a substrate with a pattern gate conductor and cap insulator, forming a dielectric masking layer having at least one opening, and, using the opening in

the dieletric masking layer as a mask, forming a trench capacitor which is self-aligned to the cap insulator edge. Chakravarti is only cited for the teaching of forming an opening in the substrate.

Accordingly, for at least the reasons discussed in Section A above, withdrawal of the rejection to claim 15 under 35 U.S.C. § 103(a) over the combination of prior art FIG. 9, Chou, Park, and Chakravarti is respectfully requested.

C. Rejection of Claim 26 under 35 U.S.C. § 103(a)

Claim 26 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over prior art Figure 9, Chou, and Park as applied to claims 1-5 above, and further in view of United States Patent No. 5,969,409, issued to Lin ("Lin"). Applicant respectfully traverses this rejection and requests reconsideration of claim 26.

Claim 26, as amended, recites a method of forming a dielectric layer in an opening, comprising forming a first dielectric layer completely filling the opening, the opening having an aspect ratio greater than about two, and forming a second and final dielectric layer over the first dielectric layer.

For at least the reasons discussed above that distinguish claims 1-5, 14, and 16-18 from the combination of teachings of prior art FIG. 9, Chou, and Park, it is believed that claim 26 is also distinguishable from FIG. 9, Chou, and Park. In particular, the "shadowing" effect illustrated in Fig. 9 prohibits the first and successive dielectric layers to fill the opening, and Chou and Park provide no teaching to address this problem.

Furthermore, it is respectfully submitted that nothing in Lin, when combined with FIG. 9, Chou, and Park, would render claim 26 obvious. Lin teaches a wafer planarization process that combines a high density plasma chemical vapor deposition (HDP-CVD) process with a chemical mechanical polishing (CMP) process. As set forth in FIG. 4, and

column 7, lines 61-65, the process employs at least three dielectric layers to form the final semiconductor devise.

Accordingly, for at least the reasons discussed above, withdrawal of the rejection to claim 26 under 35 U.S.C. § 103(a) over the combination of prior art FIG. 9, Chou, Park, and Lin is respectfully requested.

D. Rejection of Claims 6-13, 19-25, and 27-31 under 35 U.S.C. § 103(a)

Claims 6-13, 19-25, and 27-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over prior art Figure 9, Chou, and Park, as applied to claims 1-5, and further in view of United States Patent No. 5,563,104, issued to Jang et al. ("Jang"). Applicant respectfully traverses this rejection and requests reconsideration of claims 6-13, 19-25, and 27-31.

For at least the reasons discussed above that distinguish claims 1-5, 14, and 16-18, as amended, from the combination of teachings of prior art FIG. 9, Chou, and Park, it is asserted that claims 6-13, that are dependent from claim 1, are also distinguishable from FIG. 9, Chou, and Park.

Furthermore, it is respectfully submitted that nothing in Jang, when combined with FIG. 9, Chou, and Park, would render claims 6-13 obvious. Jang teaches a three-step deposition process that includes a PECVD deposition step and a two-step low and high temperature ozone-TEOS process to form a three-layered integrated circuit. Jang does not teach or suggest the present invention as recited in claims 6-13. Indeed, the Examiner on cites Jang for the teaching of forming a first and second deposition at first and second temperatures.

Accordingly, for at least the reasons discussed above, withdrawal of the rejection to claims 6-13 under 35 U.S.C. § 103(a) over the combination of prior art FIG. 9, Chou, Park, and Jang is respectfully requested.

Claims 19-25, as amended, recite a method of forming a dielectric layer in an opening, comprising forming a first dielectric layer in the opening at a first process setting, and forming a second and final dieletric layer over the first dieletric layer. At least one of the first and the second layer fills the opening, with the second layer having a top surface that is not within the opening and having a second process setting at a predetermined relationship with the first process setting.

For reasons similar to those discussed above in Sections A and C that distinguish claims 1-5, 14, and 16-18, and claim 26, respectively, from the combination of teachings of prior art FIG. 9, Chou, and Park, it is believed that claim 19-25 are also distinguishable from FIG. 9, Chou, and Park. As discussed above, FIG. 9 only describes the problems found in the prior art. FIG. 9 provides no solution to the "shadowing" effect, nor does it teach or suggest a method of filling an opening on or in a substrate through the formation of a first and second dielectric layer. The combination of teachings of prior art FIG. 9, Chou, and Park do not suggest forming a second and final dielectric layer over the first dielectric layer to fill the opening.

Furthermore, it is respectfully submitted that nothing in Jang, when combined with FIG. 9, Chou, and Park, would render claim 19-25 obvious. As discussed above, Jang teaches a three-layered integrated circuit that combines a PECVD deposition step and a two-step low and high temperature ozone-TEOS process. Jang does not teach of suggest a method of forming a semiconductor device that comprises only two dielectric layers, as recited in the claims of the present invention.

Accordingly, for at least the reasons discussed above, withdrawal of the rejection to claim 19-25 under 35 U.S.C. § 103(a) over the combination of prior art FIG. 9, Chou, Park, and Jang is respectfully requested.

Claims 27-31 each recite a method of forming a dielectric layer in an opening, that includes forming a first dielectric layer in the opening, the first layer being formed at a first process setting, and forming a second and final dielectric layer over the first dielectric layer at a second process setting, wherein at least one of the first layer and the second layer fills the opening.

Claims 27-31 have been amended in a manner similar to claims 19-25. Accordingly, for at least the reasons discussed above that distinguish claims 19-25 from the combination of teachings of prior art FIG. 9, Chou, Park, and Jang, it is believed that claims 27-31 are also distinguishable from FIG. 9, Chou, Park, and Jang. As discussed above, FIG. 9 only describes the problems found in the prior art. FIG. 9 provides no solution to the "shadowing" effect, nor does it teach or suggest a method of filling an opening on or in a substrate through the formation of a first and second dielectric layer. The combination of teachings of prior art FIG. 9, Chou, Park, and Jang to not suggest the present invention as recited in claims 27-31.

Accordingly, for at least the reasons discussed above, withdrawal of the rejection to claims 27-31 under 35 U.S.C. § 103(a) over the combination of prior art FIG. 9, Chou, Park, and Jang is respectfully requested.

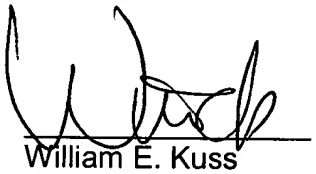
CONCLUSION

Applicant submits that claims 1-31 of the present invention recite a novel and non-obvious method of forming a dielectric layer. The cited references do not teach or suggest the claimed method. In view of the foregoing, applicant respectfully submits that the subject

application is in condition for allowance. Accordingly, reconsideration of the rejections and allowance of the claims at an early date are earnestly solicited.

If the undersigned can be of assistance to the examiner in addressing issues to advance the application to allowance, please contact the undersigned at the number set forth below.

Respectfully submitted,



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